What is claimed is:

1. A digital preemphasizer for reducing a bit-error-rate during transmission of a pulse code modulator (PCM) code on a fixed transmission line, said preemphasizer comprising:

a receiver device for receiving, in a PCM state detector, a binary PCM data input signal containing said digital PCM data and having a plurality of input address terminals and corresponding detector output terminals, for detecting a Mark-Space and Space-Mark state of each portion of said data input signal, generating a corresponding state detector signal thereof, and supplying said state detector signal at said detector output terminals;

a multiplexer controller, having a plurality of controller input terminals and a corresponding number of controller output terminals;

a receiving device for receiving at said controller input terminals said state detector signal from said detector output terminals of said PCM state detector, for generating a multiplexer control signal and a state detector control signal, supplying said state detector control signal to said controller output terminal;

a device for applying said state detector control signal to said input address terminals of said state detector for controlling said state detector;

a wide-bandwidth analog multiplexer, having a plurallity of level adjustment input terminals, a plurality of multiplexer input

terminals, and a multiplexer output terminal;

a receiving device for receiving at said multiplexer input terminals said multiplexer control signal from said controller output terminals of said multiplexer controller, for mapping said Mark-space and Space-mark state of each portion of said data input signal into a preemphasized signal comprising a constituent, adjustable amplitude for each possible said state, and supplying sais preemphasized signal at said multiplexer output terminal;

a 2X clock signal, derived from and operating at twice the frequency of the clock signal associated with said binary PCM data input signal;

a connecting device for connecting said 2x clock signal to both said multiplexer controller and said analog multiplexer, for timing and synchronizing the mapping of said Mark-space and Space-mark state of each portion of said data signal into said preemphasizer signal;

an adjustment device for generating a plurality of PCM state level adjustments, one level for each possible said Mark-space and Space-mark state, and having a corresponding number of state level adjustment output terminals with said ;level adjustments supplied thereon;

a device for connecting said level adjustments supplied at said state level adjustment output terminals to said level adjustment input terminals of said analog multiplexer, for reducing bit-error-rate of said digital PCM data by compensating for and mitigating frequency dependent attenuation intrinsic to a fixed transmission line;

a conductor device for connecting said preemphasized signal to the transmission line;

an adjustment device for providing amplitude adjustment of said preemphasized signal and impedance matching between said multiplexer output terminal of said wide-bandwidth analog multiplexer and said transmission line; and

a device for receiving, detecting, and producing a low bit-error-rate replication of said binary PCM data input signal said preemphasizer signal upon passing through said transmission line, whereby said digital preemphasizer reduces the bit-error-rate during the transmission of digital PCM data or a fixed transmission line

2. A preemphasizer, as in Claim 1, wherein said PCM state level is adjusted manually, having a plurality of individually, manually adjustable DC voltage sources, equal in number to said plurality of possible states on the PCM signal.

3. A preemphasizer, as in Claim 2, wherein said manual adjustment for PCM state level adjustment comprises a plurality of variable resistors, attached to a common source of DC voltage.

4. A preemphasizer, as in Claim 3, further comprising

a manual adjustment of said plurality of amplitude adjustment signals by observing and measuring the output signal amplitude from the wide-band amplifier of the receiver and manually, repeatedly, performing said adjustment until the amplitude is constant, indicating optimum settings for said adjustment for the

transmission line.

5. A preemphasizer, as in Claim 1, wherein said PCM state level adjustment is automatic, further comprising:

a device for producing a plurality of individually, automatically adjustable DC voltage sources, equal in number to said plurality of possible states of the PCM input signal.

6. A preemphasizer, as in Claim 4 or Claim 5, wherein said plurality of input address terminals of said PCM state detector number eighy, said plurality of possible states of said PCM signal number eight, said plurality of said state detector control signals number eight, and said plurality of preemphasizer output control signals number three.

7. A preemphasizer for reducing a bit error rate during transmission of pulse code modulator (PCM) code on a fixed transmission line, said preemphasizer comprising:

a state detector for receiving the PCM serial input signal, operatively connected thereto, and detecting a Mark or Space of each portion of the input signal thereof;

said detector means having a plurality of detector input address terminals and an equal number of detector output terminals;

a controller for providing a plurality of control signals for controlling said preemphasizer, said controller having controller input terminals, equal in number to said detector output terminals of said state detector and operatively connected thereto, said controller

having output terminals equal in number to said detector input terminals of said state detector and operatively connected thereto, said controller having a plurality of output control signals present thereon;

multiplexer for receiving said output control signals on separate multiplexer input terminals, equal in number to the plurality of said output control signals from said controller, for mapping the plurality of possible states of the PCM controller signal into a preemphasized signal comprising an adjustable amplitude for each of said possible states, having said preemphasized signal as the output signal thereof;

clock for generating a 2X clock signal, derived from and operating at twice a frequency of a clock signal of the PCM signal, operatively sending a 2X clock signal to both said controller and said multiplexer, for timing and synchronizing said mapping of the PCM signal;

a level adjustment for generating a plurality of PCM state level adjustments, one level for each of said possible states, operatively connected to said multiplexer, for mitigating frequency dependent attenuation attendant to a fixed transmission line; and

said preemphasizer signal, mapped from the PCM signal, thereon operatively connected to the input of a buffer amplifier, output of the buffer amplifier operatively connected to input of the transmission line, output of the transmission line operatively connected to a receiver, comprising a wide-band amplifier and a threshold detector thereof, the recciever producing as its output a replification of the PCM serial input signal, said preemphasizer

reducing the bit error rate during transmission of the PCM serial input signal through the transmission line.

9. A digital preemphasizer comprising:

a pulse code modulator (PCM) state detector for receiving a PCM input signal, operatively connected thereto, and detecting a Mark or Space state of each portion of the input signal, said detector having a plurality of detector input address terminals and an equal number of detector output terminals;

a multiplexer controller for providing a plurality of control signals for controlling said preemphasizer, said controller having controller input terminals, equal in number to said detector output terminals of said state detector and operatively connected thereto, said controller having output terminals equal in number to said detector input terminals of said state detector and operatively connected thereto, said controller having a plurality of output signals present thereon;

a wide-band analog multiplexer receiving said output control signals on separate multiplexer input terminals, equal in number to the plurality of said output control signals from said controller, for mapping the plurality of possible states of said PCM signal into a preemphasizer signal of adjustable and variable amplitude for each of said possible states, having said preemphasized signal as an output signal thereof;

a clock generating a wX clock signal derived from and operating at twice a frequency of a clock signal of said PCM signal,

operatively sending a 2X clock signal to both said controller and said multiplexer for timing and synchronizing said mapping of said PCM signal;

a plurality of adjustments for the PCM state level, one level for each of said possible states, operatively connected to said multiplexer for compensating for frequency dependent attenuation attendant to a fixed transmission line; and

said preemphasizer signal mapped from the PCM signal, thereupon operatively connected to the input of a buffer amplifier, output of the buffer amplifier operatively connected to the input of the transmission line, output of the transmission line operatively connected to a receiver, comprising a wide-band amplifier and a threshold detector thereof, the receiver producing as its output a replification of the PCM serial input signal, said preemphasizer reducing the bit error rate during the transmission of the PCM input signal.